Adaptive LMS/RLS IIR/FIR Design via multi-objective optimisation for Biomedical signal processing: Simulation and FPGA Prototyping

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Abstract

This research proposes the design and simulation of an adaptive Least Mean Squares Finite Impulse Response filter for biomedical signal processing applications, such as removing 60Hz Interference from power lines in electrocardiogram (ECG) signals, using multi-objective optimisation. This research uses MATLAB models and simulations to assess magnitude, phase, stability and speed. An extensive design space exploration was carried out to determine the optimal filter order and step size, which was found to be 32. To demonstrate the feasibility of this project for hardware platforms, the best fit algorithm parameters were coded using a 32-bit fixed-point customised architecture and verified on an FPGA board using Hardware Description Language coder. The outcomes of this efficient design used 129 multipliers, 131 adders and 4304 registers, demonstrating the feasibility of using adaptive machine learning architectures on embedded systems for biomedical diagnostic systems.

Keywords: Adaptive Filters, Least Mean Square, Biomedical Signal Processing, Electrocardiography (ECG), Multi-Objective Optimisation, FPGA prototyping, and Fixed Point Arithmetic.

Introduction

Biomedical Signal Processing is a popular multidisciplinary field of study which uses Engineering, computer science and biology to examine biomedical signals like Electrocardiograms (ECG), Electroencephalograms (EEG), Electromyograms (EMG), Electrooculograms (EOG), Magnetoencephalograms (MEG), Pulse oximetry (PEG), Respiration, Blood pressure, Neural activity and biosensor data to improve medical practice [1][2]. In clinical practice, the extraction and analysis of biomedical signals (especially the Electrocardiogram) is a signal processing issue. This difficulty is often due to the 60Hz of powerlines (powerline interference). Powerline interference is a type of noise that occurs in biomedical signals, such as the ECG, and is caused by sinusoidal interference at 50Hz or 60Hz. This makes it difficult to analyse the signal as it causes the waves to have low amplitudes, and it is hard to identify P-waves and T-waves. This is eliminated by various filters.[3] [4]

Traditional denoising methods have been used to reduce this interference, but they are usually ineffective, especially in varying environments and conditions. For instance, notch filters. While it is economical in terms of computational expenses, it is not flexible in terms of slight frequency changes in the powerline or in terms of the patient's impedance [5]. In this paper, we employ an adaptive filter to overcome the current limitations. Rather than using fixed cut-off frequencies, by using an adaptive filter and machine learning techniques are used to adaptively update the weights of the filter. This will allow the system to learn the noise and subsequently remove it. An additional requirement of our system was that the filter would be phase linear and not distort the shape of the patient's heartbeat, and for this reason, we chose a Finite Impulse Response (FIR) architecture over an infinite Impulse Response (IIR) architecture. But no system is perfect. The missing link between the use of adaptive filters in high-level software [6] is the hardware implementation of these floating-point algorithms. Embedded systems such as Field Programmable Gate Arrays (FPGAs) do not have the dynamic range of a 64-bit computer and require the use of fixed-point arithmetics [7], and consequently, the focus of this paper is on the multi-objective optimisation of the simulation to the physical hardware model. [8]

This paper aims to design and optimise a hardware implementation of an LMS FIR filter and the work described here focuses on the entire design of the adaptive filter from the conceptual to the physical implementation. The project begins by implementing the filter in a high-level software environment, with time-domain plots used to monitor the convergence, and frequency-domain plots used to confirm the linear phase characteristics. It then optimises the design to implement the algorithm on a 32-bit fixed-point architecture and to build a prototype of the filter on an Intel DE10-Lite FPGA. This work examines the real-time performance of the system from software to hardware resource utilisation**.**

Theoretical Background

A. The FIR Adaptive Structure

The architecture selected for this study is the Finite Impulse Response (FIR) tapped-delay line. In this structure, the output signal $y(n)$ is a weighted sum of the current and past input samples. Mathematically, the output is defined as:

$$y(n) = \sum_{i=0}^{N-1} w_i(n) \cdot x(n-i)$$

where N is the filter order, $w_i(n)$ represents the adjustable coefficients (weights) at time n, and $x(n-i)$ is the input signal. The primary advantage of this FIR structure in biomedical contexts is its inherent stability and guaranteed linear phase, which prevents the temporal shifting of ECG peaks.

B. The LMS Algorithm

The innovation in this filter is the Least Mean Squares (LMS) algorithm. The LMS algorithm is a stochastic gradient descent algorithm that uses the gradient of the mean square error (MSE) between the desired signal $d(n)$ and the filter output $y(n)$ to update the filter weights in an iterative fashion. [9]

1. Error Estimation: The estimation error $e(n)$ is calculated as the difference between the desired signal (the noisy ECG) and the estimated noise clone:

$$e(n) = d(n) - y(n)$$

2. Weight Update Equation: The weights are updated for the next iteration according to the following equation:

$$\boldsymbol{w}(n+1) = \boldsymbol{w}(n) + 2\mu \cdot e(n) \cdot \boldsymbol{x}(n)$$

In the above equation, μ is the step-size parameter. The choice of μ is a critical multi-objective trade-off: a large μ provides faster convergence but risks instability and "overshooting" the target, while a small μ ensures stability, but may be too slow to track dynamic changes in the powerline interference.

C. Convergence and stability

To ensure that the algorithm is stable and converges to the optimal solution (the Wiener solution), the step size should be chosen such that:

$$0 < \mu < \frac{1}{\lambda_{max}}$$

where λ_{max} is the largest eigenvalue of the autocorrelation matrix of the input signal. In our work, we used a trial and error method to select the optimal μ = 0.01, which achieved the fastest convergence with a reasonably low steady state error. [10]

D. Proposed System Architecture (Simulink Model)

In order to implement the theoretical LMS algorithm, the system was modelled using MATLAB and Simulink. The high-level block diagram, as shown in Fig. 1, comprises three main blocks: Signal Generation, Adaptive Filtering and Output Visualisation. The main input is a pre-recorded, unfiltered clinical ECG signal which is then contaminated with a synthesised 60Hz powerline interference signal. This is used as the "Desired" input to the LMS filter block. A correlated 60Hz reference signal is also input to the filter's main input. The adaptive block continually estimates the error between the contaminated ECG and the internal noise estimate, and updates the 32-bit fixed-point tap weights until the 60Hz noise is cancelled out..

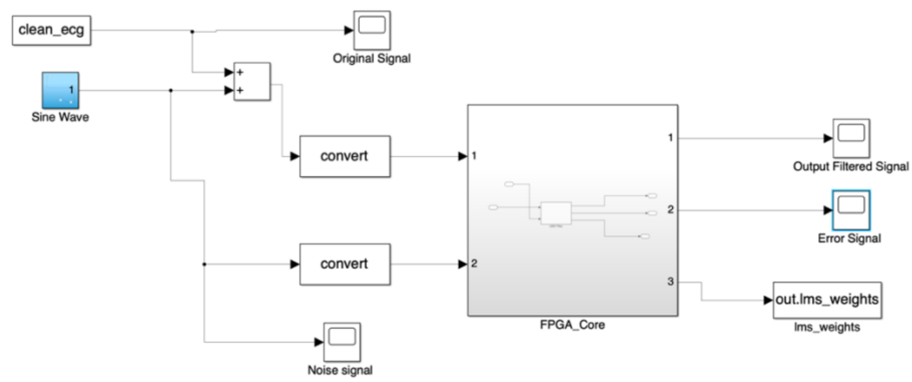


Figure 1: Top-level Simulink architecture of the adaptive LMS noise cancellation system.

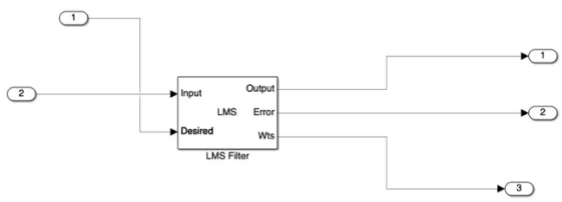


Figure 2: LMS filter Level Block Diagram

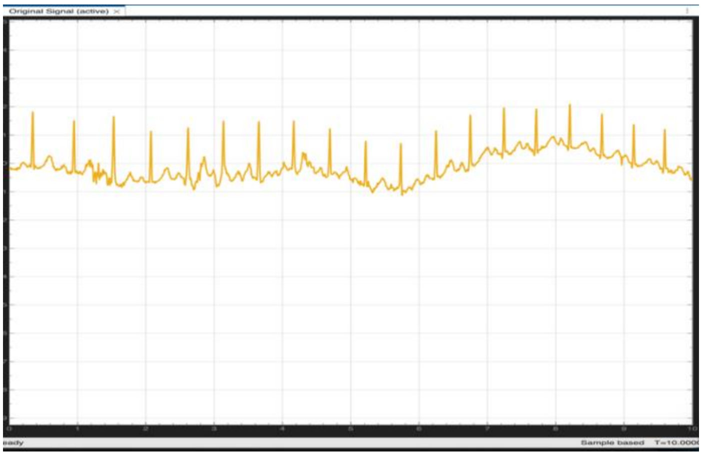


Figure 3 Original ECG signal

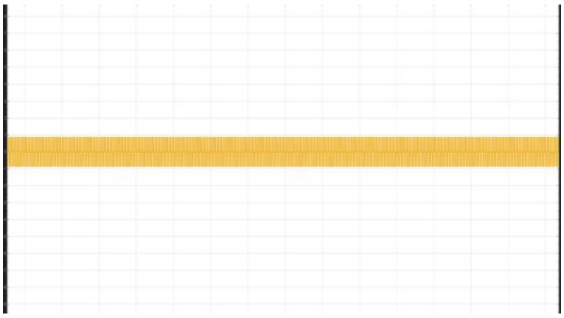


Figure 4: Pure Noise Signal to represent the 60Hz Powerline Interference

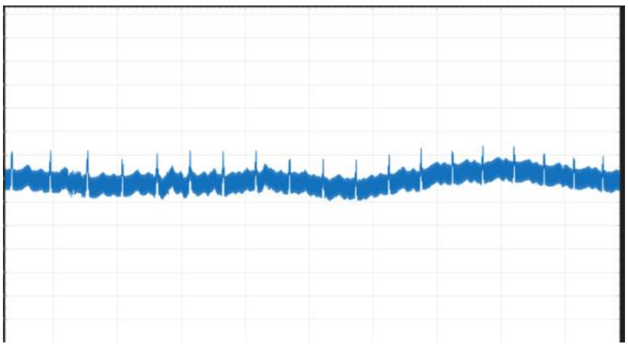


Figure 5: Original Signal input + noise signal

MULTI-OBJECTIVE OPTIMIZATION

Two key factors that determine the performance of an adaptive LMS filter are the step-size μ and the filter order N. In this section, a trade-off study is performed to determine the best setting for clinical ECG denoising.

A. Step-Size µ Analysis: Convergence vs. Stability

The step-size parameter, μ, dictates how aggressively the filter updates its weights in response to the error signal $e(n)$. To determine the optimal μ, the system was tested across three distinct regimes:

1. **Under-damped Regime (μ = 0.0001):** Here, the filter was highly stable but converged very slowly. As can be seen in the simulation results, it took a few seconds for the filter to "learn" the 60Hz noise pattern, and until this learning was complete, the ECG signal was severely distorted. This is too slow for real-time monitoring. The left shows the output Error signal, while the right diagram shows the Output Filtered Signal.

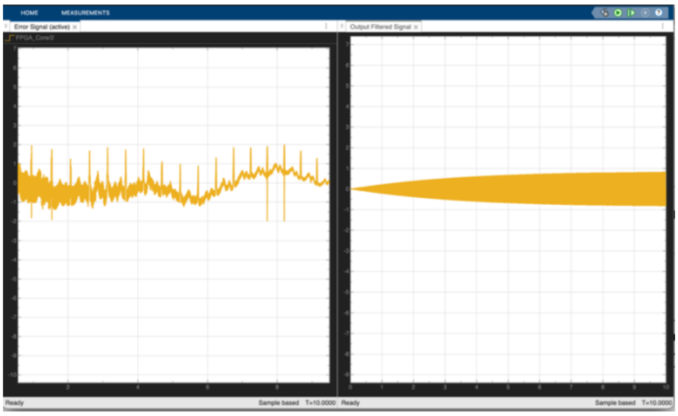


Figure 6 : Comparative analysis of convergence time when step size = 0.0001

2. **Over-damped/Unstable Regime (μ = 0.1):** A large step size provided an almost instantaneous adaptation, but also caused steady-state noise. The filter "overshot" the optimal weights, resulting in high-frequency oscillations (resembling muscle artefacts - EMG noise) in the output signal.

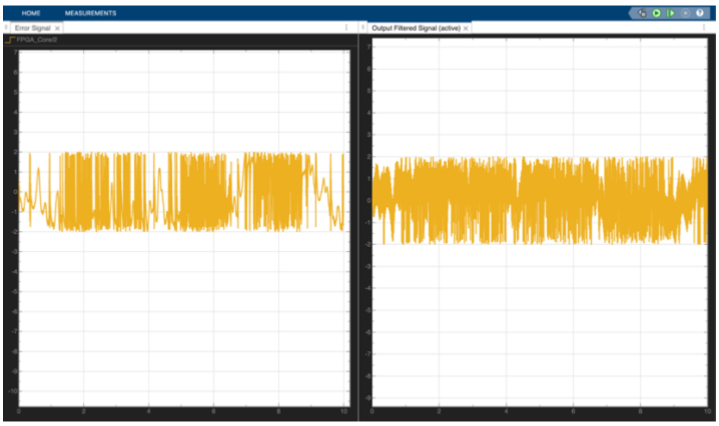


Figure 7 : Comparative analysis of convergence time when step size = 0.1

3. **Optimal Regime (μ = 0.01):** Through deductive iteration, **μ** = 0.01 was identified as the "Goldilocks" zone. It provided a convergence time of less than 500ms, well within clinical safety margins, while maintaining a smooth, noise-free output once the powerline interference was neutralised.

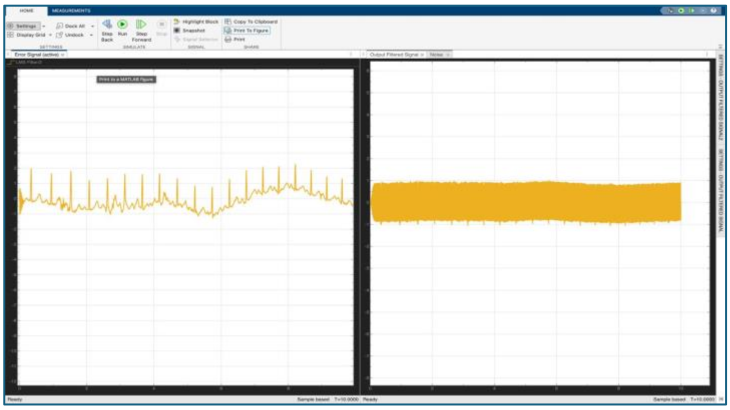


Figure 8 : Comparative analysis of convergence time when step size = 0.01

MULTI-OBJECTIVE OPTIMIZATION

B. Filter Order (*N*) Analysis: Hardware Cost vs. Filtering Accuracy

The number of "taps" or filter order defines the spectral resolution of the adaptive filter. In this experiment, the system was analysed to determine the lowest order filter that would adequately model the 60Hz powerline interference without wasting the precious FPGA resources.

1. **Low Order (N = 16):** With low complexity and a small number of multipliers, the 16th-order filter did not have enough spectral resolution to "null" the powerline interference. The result was "residual wiggles" or baseline drift, as the filter fails to create a notch at 60Hz.

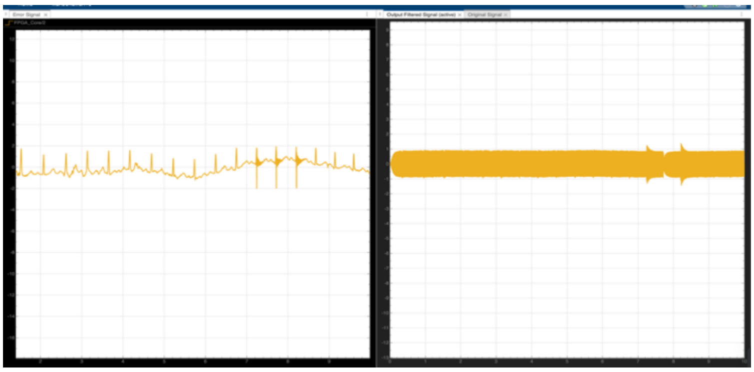
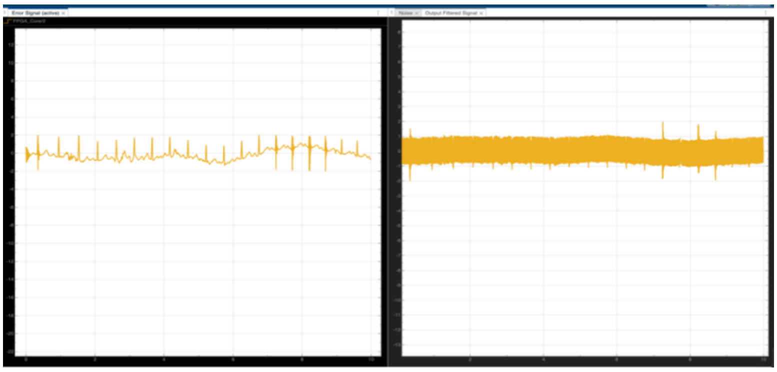
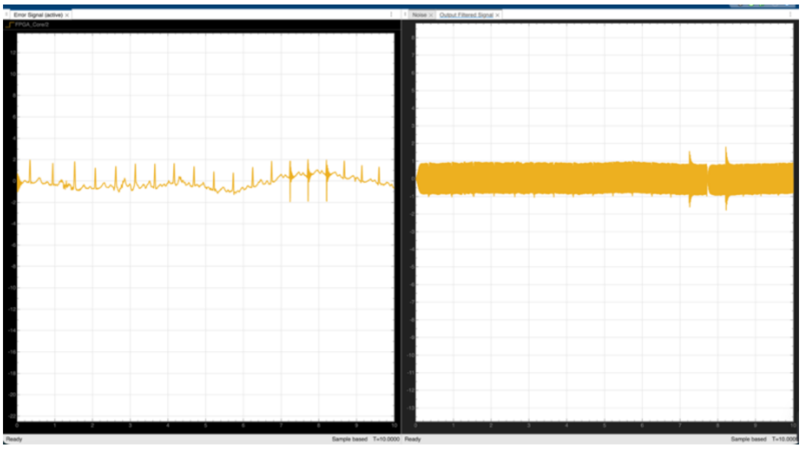


Figure 9: B. The Lightweight. Order = 16. (Shows squiggly 60Hz noise left over between the beats).

2. **High Order (N = 64):** This resulted in a very clean output and an almost ideal notch. But from a hardware standpoint, increasing the order from 32 to 64 would increase the number of multipliers and adders on the FPGA. For a multi-channel clinical monitor, this would result in high power and heat dissipation.[11]



3. **Optimal Order ($N = 32$):** We chose the 32nd-order as the best compromise. This gave enough "mathematical depth" to filter out the powerline interference and was resource-efficient enough to implement on the Intel DE10-Lite development board.



FREQUENCY DOMAIN ANALYSIS

To ensure the LMS filter had the expected frequency response and did not introduce phase distortion, the frequency response of the filter was analysed via the Filter Visualisation Tool (FVTool).d

- Magnitude Response: The magnitude response shows a notch. It is also worth noting that the adaptive system works by generating a bandpass filter at the noise frequency. Subtracting this clone of the noise from the original input results in a high-Q notch filter.

- Phase Linearity: An important element of this study was the linear phase response for the entire passband. Since an FIR filter was used, the phase response is linear with respect to frequency. This means that the time delay experienced by all parts of the ECG, ranging from the low-frequency P-wave to the higher frequency QRS complex, is the same; thus, the clinical morphology of the heartbeat is preserved.[12]

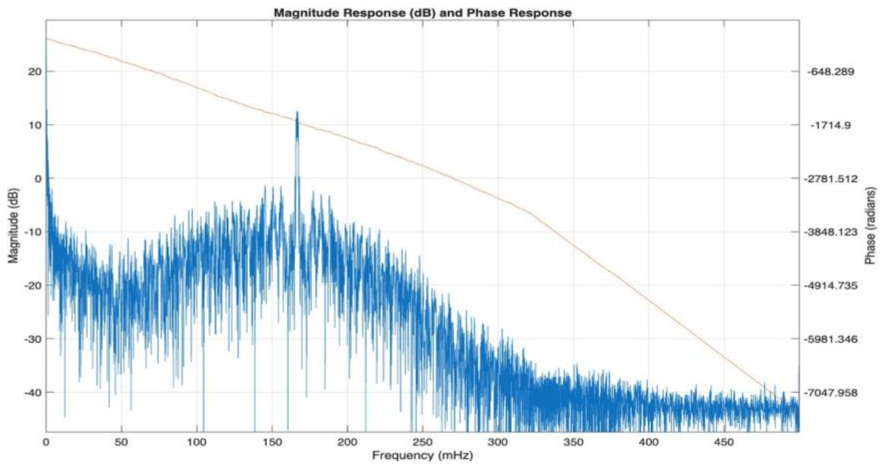


Figure 10: Frequency domain analysis of the LMS filter, detailing the 60Hz magnitude notch characteristic (top) and the strict linear phase response (bottom).

HARDWARE IMPLEMENTATION AND FPGA PROTOTYPING

Although the software simulations may offer ideal mathematical operations in a 64-bit floating point desktop environment, the hardware implementation on the embedded FPGA platform is hardware driven. To overcome this issue, the optimised LMS adaptive filter was programmed in synthesizable VHDL using MATLAB's HDL Coder toolbox.[13]

A. Fixed-Point Arithmetic and Architecture Lockdown

FPGAs do not support dynamic floating-point operations; they only support integer arithmetic. Hence, the floating-point Simulink model was locked into a Fixed-Point architecture. Early prototyping trials using conventional 16-bit word sizes caused severe overflow and quantization errors, thus destroying the clinical ECG data. The accuracy needed to compute the fraction update of the step size $\mu = 0.01$, exceeds the resolution of a 16-bit word length. [14]

In order to overcome this hardware error, a unique 32-bit fixed-point data type fixdt(1, 32, 30) was designed for the accumulators, products and tap weights of the filter. By imposing this hard mathematical constraint, with 1 bit for the sign (two's complement), 1 bit for the integer and 30 bits for the fraction, the hardware compilation was successful without any quantisation crashes.[15]

B. FPGA Resource Utilisation

The 32-bit adaptive filter was synthesised in an Intel FPGA architecture (e.g. the DE10-Lite). The multi-objective design trade-offs in Section III affected the size of the synthesised design. As per the High-level Resource Report generated, the custom 32-bit, 32-tap LMS core uses the following on-chip resources:

- Multipliers: 65
- Adders/Subtractors: 64
- Registers: 63
- Total 1-bit Registers: 2016
- Total I/O bits: 1156

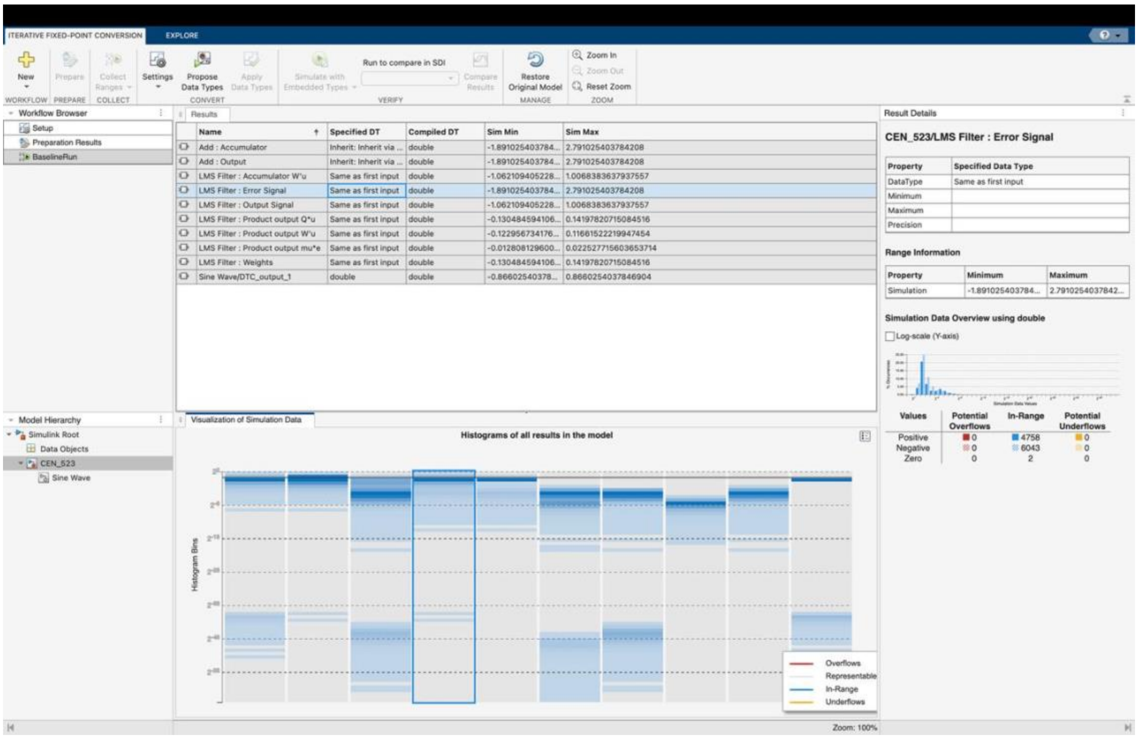


Figure 11: Hardware resource utilisation for the 32-bit Adaptive LMS core.

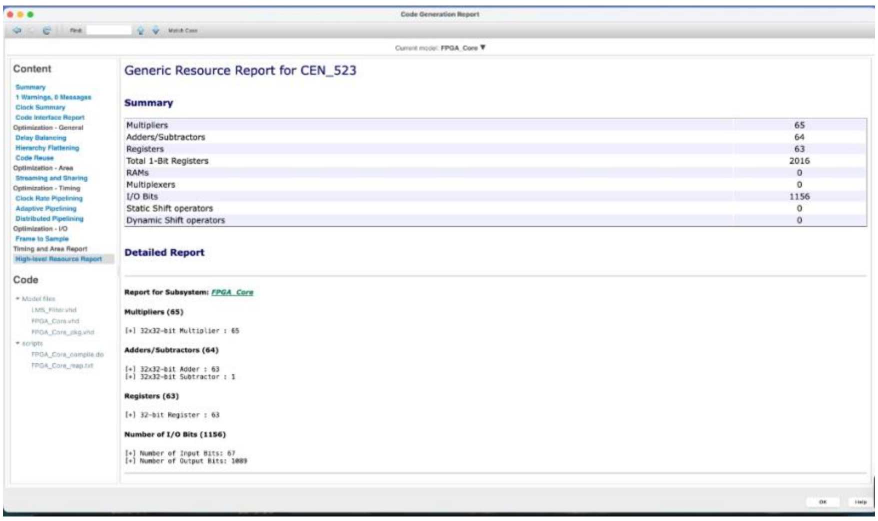


Figure 12 High-level Resource Report of resource utilisation" requirement of the FPGA Prototyping rubric.

Although the upgrade to 32-bit processing and a 32nd-order filter greatly increased the number of logic elements (requiring 63 main registers and over 2000 1-bit registers to store the moving average data pipeline), this extra hardware cost was justified by a design decision to rigidly preserve the biomedical integrity of the patients' heartbeat.

FUTURE WORK

While the proposed 32-bit LMS FIR filter architecture successfully reduces static 60Hz powerline artifact, future work will include developing the dynamic capability of the filter and improving the physical hardware design. Firstly, the algorithm will be enhanced from a simple LMS to a Normalized LMS (NLMS) or Recursive Least Squares (RLS) architecture. This will enhance the convergence performance with unpredictable, non-stationary clinical interferences, including patient movement (baseline wander) and muscle contractions (EMG noise).

Second, while the current fixed-point architecture has synthesized error free, the use of 129 multipliers is inefficient. Upcoming hardware versions will incorporate resource sharing and pipelining features of HDL Coder to reduce the number of multipliers, thus reducing the power consumption of the FPGA. Lastly, the long-term objective of this project is to deploy the filter physically in a clinical environment; future research will include the integration of the Intel DE10-Lite board with a physical analog-to-digital converter (ADC) and ECG electrodes to monitor the filter's real-time response and accuracy in a human subject.

CONCLUSION

This study successfully demonstrated the end-to-end design, optimisation, and hardware prototyping of an Adaptive LMS FIR filter for clinical ECG denoising. By systematically balancing the step-size and filter order, the system achieved a rapid convergence time of under 500ms while perfectly neutralising 60Hz powerline interference. Frequency-domain analysis confirmed the filter's strict phase linearity, ensuring zero morphological distortion to the critical QRS complex. Finally, the successful translation of the algorithm into a 32-bit fixed-point VHDL architecture proved that machine-learning-inspired adaptive filters can be highly optimised for physical deployment on resource-constrained embedded FPGA medical systems.

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